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a) the 32-bit parallel current state of LFSR bits Ifsr(58) down to Ifsr(27); and ... else
{ /* scramble data with current scrambler state */ ...
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This is rather simple, all you do is have an 43 bit LFSR, that is loaded with the data in parallel and scramble in parallel. in VHDL: ... www.opencores.org/forums/cores/2004/04/000639 - 22k - Cached - Similar pages

Cryptography-Digest Digest #543

The common technique as John Savard suggested is to use an LFSR to provide ... I have a project where we need to scramble (and unscramble) a parallel data ... www.mail-archive.com/cryptography-digest@senator-bedfellow.mit.edu/msg01749.html - 51k - Cached - Similar pages

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Test Data Decompression for Multiple Scan Designs with Boundary Scan 8 C. Dufaza and G. Gambon, "LFSR-Based Deterministic and Pseudo-Random Test ... 16 J. Rajski and J. Tyszer, "A Parallel Decompressor and Related Methods and ... portal.acm.org/citation.cfm? id=305088&jmp=indexterms&coll=GUIDE&dl=GUIDE&CFID=3962266&... - Similar pages

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Combining dictionary coding and LFSR reseeding for test data compression, ...

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[PS] Cryptanalysis of MUX-LFSR Based Scramblers

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the representation of Sect.2 there are 256 parallel generators, one for every ...
corresponds to the generation of the MSB bit of a 8-bit word to scramble ...
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[Paper] The Algorithm of 16-Bit Scrambler in Parallel for PCI Express
KEY WORDS Scramble(r), De-scramble(r), PCI Express, Linear Feedback Shift
Register (LFSR) 1. Introduction PCI Express technology is one of new serial I/O ...
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indication to bypass the scrambler and hold the present state of the linear feedback
shift register. /* Parallel Scrambler Implementation for: */ ...
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high-speed applications. A new DET D-register with embedded. XOR. operation is used as a basic circuit block of the parallel scram- ... ieeexplore.ieee.org/iel5/8920/34715/01658189.pdf? isnumber=34715&prod=JNL&arnumber=1658189&arS... - Similar pages

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If a machine can perform two MAC operations in parallel, the loop in the ... determines the feedback taps of linear-feedback-shift-register (LFSR) and ... portal.acm.org/citation.cfm?doid=644254.644267 - Similar pages

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And the long PN code is also used in the **scramble** for a forward link and in the ...
Generally a cyclic code is calculated using a **feedback register** ...
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To make such information secret, a **scramble** encoder having a scrambling function is ... The PN generator 27 is composed of a **feedback** shift **register** for ... gauss.ffii.org/PatentView/EP620690 - 59k - <u>Cached</u> - <u>Similar pages</u>

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These parallel operations are well suited to hardware VLSI implementation. ... shift register with feedback) augmented by an extra 0 to make 64 bits. ... www.qsl.net/n9zia/newlinkpaper.html - 52k - Cached - Similar pages

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Integer. Load/Store. Branch. Vector. Vector (DLP). 4 data parallel operations ...
Separate architected register spaces (e.g. Integer, Vector, Accumulator) ...
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If a machine can perform two MAC operations in parallel, the loop in the ... which repeats a complex, bit-oriented step 16 times to scramble 64 bits of data ... acmqueue.com/modules.php?name=Content&pa=showpage&pid=40&page=2 - 59k - Cached - Similar pages

<u>Project: IEE802.3z Gigabit Ethernet Task Force Source: Steve ...</u> **Scramble** the entire frame excluding the preamble bytes using a self ... Using 2 identical implementations **operating** in **parallel**, **operation** at 1Gbps using 2 ... grouper.ieee.org/groups/802/3/z/public/presentations/sep1996/BHgutp_b.txt - <u>Similar pages</u>

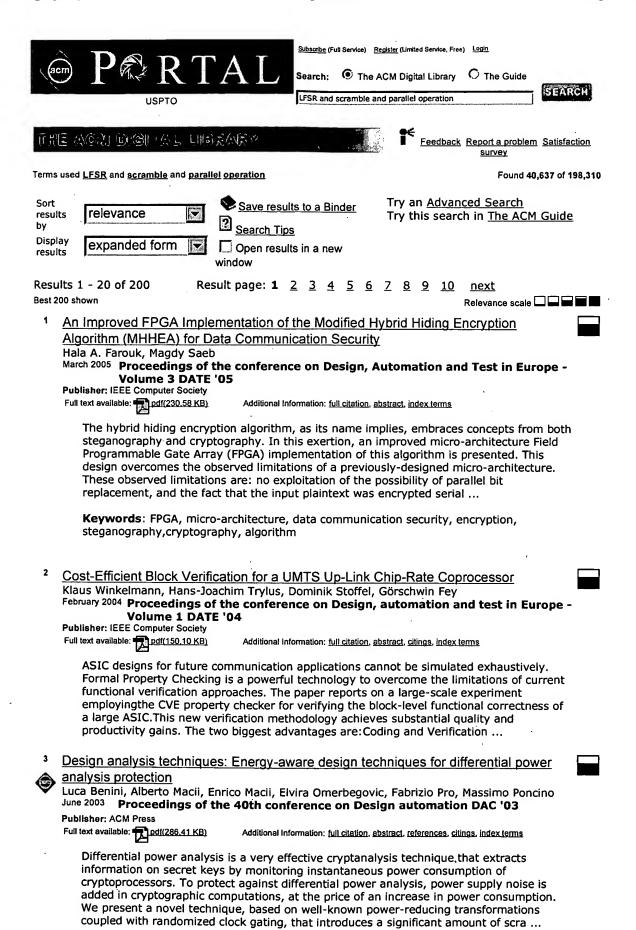
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The placement of the XOR feedback terms is mathematically defined by a ... and their outputs feed back to the shift register input to scramble and feed ... books.google.com/books?isbn=0071409270...

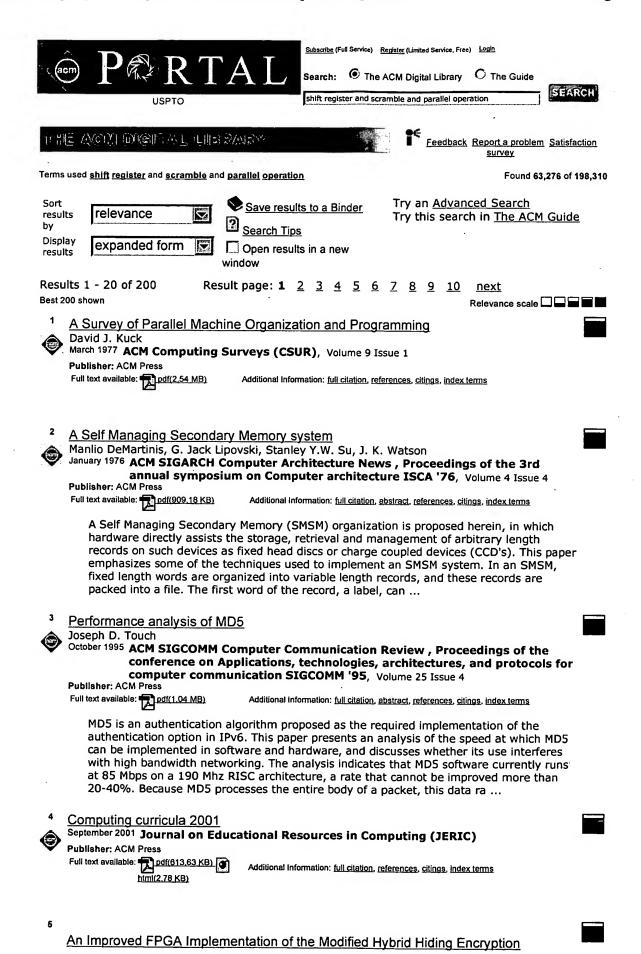
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the irdeto softclient is required to register securely with the Plsys ... scramble 140
streams (mPeG-2 at 4.5 mb/s) in parallel with a single iP scrambler. ...
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Memory is implemented as feedback register banks or dual-port ... redirect data
through the convolutional encoder (decoder) or it can scramble ...
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Algorithm (MHHEA) for Data Communication Security

Hala A. Farouk, Magdy Saeb

March 2005 Proceedings of the conference on Design, Automation and Test in Europe -Volume 3 DATE '05

Publisher: IEEE Computer Society

Full text available: pdf(230.58 KB)

Additional Information: full citation, abstract, index terms

The hybrid hiding encryption algorithm, as its name implies, embraces concepts from both steganography and cryptography. In this exertion, an improved micro-architecture Field Programmable Gate Array (FPGA) implementation of this algorithm is presented. This design overcomes the observed limitations of a previously-designed micro-architecture. These observed limitations are: no exploitation of the possibility of parallel bit replacement, and the fact that the input plaintext was encrypted serial ...

Keywords: FPGA, micro-architecture, data communication security, encryption, steganography, cryptography, algorithm

LIPP - a SIMD multiprocessor architecture for image processing

T. Ericsson, P. E Danielsson

June 1983 ACM SIGARCH Computer Architecture News, Proceedings of the 10th annual international symposium on Computer architecture ISCA '83. Volume

11 Issue 3

Publisher: IEEE Computer Society Press, ACM Press

Full text available: pdf(563.81 KB)

Additional Information: full citation, abstract, references, citings, index terms

LIPP (Linköping Image Parallell Processor) is a multiprocessor system intended mainly for image analysis and image processing but even other computing tasks where large amount of data should be manipulated in forms of matrices, such as weather forecasts or other related problems namely systems of differential equations. The processors within the processor array are of bit-serial type with the capability of directly processing data with wordlengths in the range of 1 bit to 32 bits in on ...

The state of the art in distributed query processing



Donald Kossmann

December 2000 ACM Computing Surveys (CSUR), Volume 32 Issue 4

Publisher: ACM Press

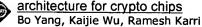
Full text available: pdf(455.39 KB)

Additional Information: full citation, abstract, references, citings, index terms

Distributed data processing is becoming a reality. Businesses want to do it for many reasons, and they often must do it in order to stay competitive. While much of the infrastructure for distributed data processing is already there (e.g., modern network technology), a number of issues make distributed data processing still a complex undertaking: (1) distributed systems can become very large, involving thousands of heterogeneous sites including PCs and mainframe server machines; (2) the stat ...

Keywords: caching, client-server databases, database application systems, dissemination-based information systems, economic models for query processing, middleware, multitier architectures, query execution, query optimization, replication, wrappers

Advances in design-for-testability methods: Secure scan: a design-for-test



June 2005 Proceedings of the 42nd annual conference on Design automation DAC '05

Publisher: ACM Press

Full text available: pdf(234.65 KB)

Additional Information: full citation, abstract, references, index terms

Scan-based Design-for-Test (DFT) is a powerful testing scheme, but it can be used to retrieve the secrets stored in a crypto chip thus compromising its security. On one hand, sacrificing security for testability by using traditional scan-based DFT restricts its use in privacy sensitive applications. On the other hand, sacrificing testability for security by abandoning scan-based DFT hurts product quality. The security of a crypto chip comes from the small secret key stored in a few registers and ...

Keywords: crypto hardware, scan-based DFT, security, testability

Scalable high-speed prefix matching



Marcel Waldvogel, George Varghese, Jon Turner, Bernhard Plattner

November 2001 ACM Transactions on Computer Systems (TOCS), Volume 19 Issue 4

Publisher: ACM Press

Full text available: pdf(933.02 KB)

Additional Information: full citation, abstract, references, citings, index terms

Finding the longest matching prefix from a database of keywords is an old problem with a number of applications, ranging from dictionary searches to advanced memory management to computational geometry. But perhaps today's most frequent best matching prefix lookups occur in the Internet, when forwarding packets from router to router. Internet traffic volume and link speeds are rapidly increasing; at the same time, a growing user population is increasing the size of routing tables against which p ...

Keywords: collision resolution, forwarding lookups, high-speed networking

A tutorial on uniform variate generation



P. L'Ecuyer

October 1989, Proceedings of the 21st conference on Winter simulation WSC '89

Publisher: ACM Press

Full text available: pdf(777.59 KB)

Additional Information: full citation, abstract, references, citings, index terms

In typical stochastic simulations, randomness is produced by generating a sequence of independent uniform variates (usually real-valued between 0 and 1, or integer-valued in some interval) and transforming them in the appropriate way. In this tutorial, we examine practical ways of generating such variates on a computer. We compare them in terms of ease of implementation, efficiency, flexibility, theoretical support, and statistical robustness. We look in particular at the following classes of ge ...

11 Wireless communication and networking: ASIP architecture for multi-standard wireless terminals



D. Lo Iacono, J. Zory, E. Messina, N. Piazzese, G. Saia, A. Bettinelli March 2006 Proceedings of the conference on Design, automation and test in Europe:

Designers' forum DATE '06 Publisher: European Design and Automation Association

Full text available: pdf(799.10 KB)

Additional Information: full citation, abstract, references

This paper presents the Block Processing Engine (BPE), an Application Specific Instruction-Set Processor (ASIP) explicitly designed for the implementation of multi-standard wireless terminals. Thanks to a high level of parallelism and a consistent use of pipeline, the BPE architecture fully satisfies stringent real-time constraints imposed by emerging technologies. Its efficiency has been proven through the implementation, the physical synthesis for the CMOS 90nm STM technology and the FPGA prot ...

Partial reconfigurable architectures: Task scheduling for heterogeneous



reconfigurable computers

Ali Ahmadinia, Christophe Bobda, Dirk Koch, Mateusz Majer, Jürgen Teich September 2004 Proceedings of the 17th symposium on Integrated circuits and system design SBCCI '04

Publisher: ACM Press

Full text available: pdf(131,32 KB)

Additional Information: full citation, abstract, references, index terms

We consider the problem of executing a dynamically changing set of tasks on a reconfigurable system, made upon a processor and a reconfigurable device. Task execution on such a platform is managed by a scheduler that can allocate tasks either to the processor or to the reconfigurable device. The scheduler can be seen as part of an operating system running on the software or as core in the reconfigurable device. For each tasks to be executed on reconfigurable device, an equivalent implementation ...

Keywords: FPGA, hardware preemption, partial reconfiguration, placement, reconfigurable computing, scheduling

Architectural features of CASSM: A Context Addressed Segment Sequential Memory G. J. Lipovski April 1978 Proceedings of the 5th annual symposium on Computer architecture ISCA

